High-level Synthesis Methods on FPGA-s

1. SYLLABUS INFORMATION

1.1. Course title
High-level Synthesis Methods on FPGA-s

1.2. University
Pázmány Péter Catholic University

1.3. Semester
1st year, 1st semester

2. COURSE DETAILS

2.1. Course nature
Elective

2.2. ECTS Credit allotment
5

2.3. Faculty data
Dr Zoltán Nagy

3. COMPETENCES AND LEARNING OUTCOMES

3.1. Course objectives
The purpose of the course is to introduce basic signal processing techniques relevant to biomedical signals and illustrate their practical applications.

3.2. Course contents
Digital circuits have traditionally been designed using specialized hardware description languages like VHDL and Verilog at the Register Transfer Level (RTL). However, the increasing complexity of modern digital systems demands more efficient and flexible design methodologies. High-Level Synthesis (HLS) methods, which have been an active research area since the 1980s, have now matured for use in industrial applications. Unlike traditional VHDL-based design flows, the input to an HLS synthesis system is a standard ANSI C/C++ description, and the structure of the synthesized architecture can be defined using compiler directives. By modifying these directives, less design effort and much shorter time are required to generate several different architectures for the same algorithm. During design space exploration, the area, speed, power dissipation, and memory bandwidth parameters of the different solutions can be compared, allowing the best option to be selected for a particular implementation.

Detailed Course Contents

1. Introduction to HLS flow, binding, allocation, scheduling, and control path generation
2. Overview of field-programmable system-on-chip (SoC) architectures, focusing on the Xilinx Zynq architecture
3. Modeling arbitrary-width data types in C/C++
4. The ARM AMBA AXI-4 bus system
5. Simulation and on-chip verification
6. Interface synthesis, interface types, and control signals
7. Synthesis of arrays, array transformations, and handling dependencies

8. Synthesis of loops I: Pipelining
9. Synthesis of loops II: Unrolling
10. Synthesis of functions and hierarchical designs
11. AXI DMA infrastructure IP cores
12. Hardware/software partitioning
13. Case Study I: Image processing system
14. Case Study II: Smith-Waterman algorithm
15. Case Study III: Solving partial differential equations

3.3. Course bibliography

Required reading:

Michael Fingeroff, “High-Level Synthesis Blue Book”, Xlibris, 2010
Philippe Coussy, Adam Morawiec, "High-Level Synthesis: from Algorithm to Digital Circuit", Springer, 2008
Louise Crockett, Ross Elliot, Martin Enderwitz, Bob Stewart, David Northcote, "The Zynq Book Tutorials for Zybo and ZedBoard", Strathclyde Academic Media, 2015
Xilinx Vivado Design Suite User Guide: High-Level Synthesis
Xilinx Vivado Design Suite Tutorial: High-Level Synthesis

Recommended reading:

Raul Camposano and Wayne Wolf, eds., “High-Level VLSI Synthesis”, Springer, 1991.
Sumit Gupta, Rajesh Gupta, Nikil D. Dutt, Alexandru Nicolau, "SPARK: A Parallelizing Approach to the High-Level Synthesis of Digital Circuits", Springer, 2004

4. TEACHING AND LEARNING METHODOLOGIES AND STUDENT WORKLOAD

4.1. Contact hours

- Lecture: 2 hours/week
- Practice: 0 hour/week
- Lab: 2 hours/week

5. EVALUATION PROCEDURES AND WEIGHT OF COMPONENTS IN THE FINAL GRADE

5.1. End-term evaluation

End-term evaluation: written and oral exam